REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated September 22, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-16 are under consideration in this application. Claims 1-4 and 6-15 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention.

Additional Amendments

The specification, the drawings, and the claims are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification as noted in parentheses as follows.

A data processing device of the invention, as now recited in claim 1, including a set-associative cache memory capable of performing associative operation by sequentially comparing tag information contained in an access address signal with tag information contained in each of ways of a cache line (p. 7, lines 13-19; p. 18, lines 24-28) which is selected as an information storage area with lower bits of the access address signal (p. 18, lines 14-20; p. 20, lines 8-13). The cache memory comprising: way prediction means 13 for predicting one of the ways of the cache line as a matching way in parallel with the associative operation; generation means 30 for generating way selection determining information 23 based on the associative operation using a subsequent access address signal during a penalty cycle which is caused by a prediction miss of said way prediction means (p. 22, lines 4-13); and control means 31 (Fig. 1), 31A (Fig. 11) for selecting one of the ways of a cache line, which is selected as an information storage area with lower bits of the subsequent access address signal, as a matching way for the subsequent access address signal after the penalty cycle using the way selection determining information 23 (p. 22, lines 13-27).

IN THE DRAWINGS:

Please enter the attached corrected drawings Figs. 4-10, wherein in Fig. 4, "ANY WAY IS HIT?" is being changed into "SELECTED WAY IS CACHE HIT?", and in Figs. 5-10, "WAY SELECT" is being changed into "WAY SELECTED", to replace Figs. 4-10 as originally filed. A Letter to Draftsperson is also submitted herewith.

Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

The title, specification including abstract, and claims 1-16 were objected to for informalities, and the Examiner has requested correction thereof. Claims 1-16 were rejected under 35 U.S.C. § 112, first paragraph, for claiming an invention which is not described in the specification in a manner that will enable a skilled person in the art to make or use the invention, and claims 1-16 were further rejected under 35 U.S.C. § 112, second paragraph, as being indefinite in claiming the invention.

The claims and drawings are being amended as required by the Examiner to overcome the informality rejections. In particular, regarding the enablement rejection, claim 1 is fully supported and enabled by the specification in view of the prior art references as noted in parentheses as the Additional Amendments portion. In addition, an article entitled "Reducing Set-Associative Cache Energy via Way-Prediction and Selective Direct-Mapping" by Michael D. Powell presented during December 01 - 05, 2001 is concurrently submitted via IDS as general background information of the art, although it was only available after the priority date of April 27, 2001, of the invention

Regarding the Examiner's request for a substitute specification, Applicants respectfully contend the revised portions of the specification in conjunction with the amended claim 1 sufficiently addresses the Examiner's confusion, especially regarding what is being done in the associative operation in parallel with way prediction. As such, the need for a substitute specification is eliminated.

Accordingly, the withdrawal of all outstanding informality rejections is in order, and is therefore respectfully solicited.

Prior Art Discussion

Although the Examiner has not yet applied the cited prior art against the invention, these references have been carefully considered, but are most respectfully traversed as follows.

The data processing device including a set-associative cache memory capable of performing associative operation of the invention, as now recited in independent claims 1, 4 and 8, selectively utilize the way prediction under different circumstances, i.e., switchably

operating under a first operation mode for selecting a matching one of ways of a cache line according to a result of the associative operation and a second operation mode for predicting a matching one of ways of a cache line based on prediction conducted in parallel with the associative operation (claim 4). In particular, when the way prediction fails (i.e., a prediction miss of said way prediction means), the invention uses way selection determining information based on the associative operation to select a matching way instead, during/after a penalty cycle (claims 1 and 8). As such, the invention prevents successive way misses incurred by a prediction miss.

Applicants respectfully contend that none of the cited prior art references teaches or suggests "using way selection determining information based on the associative operation to select a matching way during/after a penalty cycle thereby preventing successive way misses incurred by a prediction miss" according to the invention.

In contrast, the cited prior art references merely disclose the general way prediction, rather than any mechanism countering a way perdition miss.

Applicants contend that neither the cited prior art references, nor their combinations teaches or discloses each and every feature of the present invention as recited in independent claims 1, 4 and 8. As such, the present invention as now claimed is distinguishable and thereby allowable over the prior art as a whole.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference. Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance

of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

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